ANALYSIS OF SENSE AMPLIFIER CIRCUIT USED IN HIGH PERFORMANCE & LOW POWER SRAM

[1*]Anangaraj Singh
Dept. of Electronics and Communication Engineering
M.M.M. University of Technology
Gorakhpur, India
Email: anangaraj107@gmail.com

[2]Dr.R.K.Chuhan
Dept. of Electronics and Communication Engineering
M.M.M. University of Technology
Gorakhpur, India
Email: rkchauhan27@gmail.com

ABSTRACT: Large bit-line capacitance is one of the main bottlenecks to the performance of on-chip caches. New sense amplifier techniques need to explicitly address this challenge. This paper describes three sensing techniques to overcome this problem: a voltage sense amplifier (VSA), a current sense amplifier (CSA) and a charge transfer sense amplifier (CTSA). Increased process variation and reduced operating voltage present two of the main challenges in using sense amplifiers for small geometry bulk CMOS process technology. The current sense amplifier senses the cell current directly and shows a speed improvement as compared to the conventional voltage mode sense amplifier, for same energy. The other is a charge transfer sense amplifier that takes advantage of large bit-line capacitance for its operation. CTSA shows an improvement for read delay and consumes less energy than the voltage mode sense amplifier. CTSA results in reduced bit-line swing and which in turn leads to lower bit-line energy than the conventional voltage mode.

Key words: CMOS, SRAM, VSA, CSA, CTSA, BIT-LINE.

Introduction

Static Random Access Memories (SRAMs) are an important component of microprocessors and system-on-chips. SRAMs are used as large caches in microprocessor cores and serve as storage in various IPs on a system-on-chip.SRAMs used in high performance microprocessors and graphics chips have high speed requirements. At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. Since SRAMs serve as large storage on these chips, it's very important to get maximum density out of these. Traditionally a large number of SRAM bit cells, up to 1024 in some cases, are connected to a common bit-line to get the highest density and array efficiency. This results in a large capacitance on the bit-lines which necessitates using differential sense amplifiers for speed reasons. Sense amplifiers detect the data being read by sensing a small differential voltage swing on the bit-lines rather than waiting for a full rail-to-rail swing.

Depending on the performance and power requirements, it's very important for the sense amplifiers to operate fast and do so while burning a minimum amount of power. The large bit-line capacitance is a big performance bottleneck.

Conventional Voltage Sense Amplifiers need a minimum amount of differential voltage to be developed on the bit-lines for reliable operation. The amount of time required to develop this differential voltage is linearly proportional to bit-line capacitance. The dynamic power consumed in pre-charging the bit-lines increases with the differential voltage that needs to be developed. Low power requirements of mobile and embedded chips require sense amplifiers which burn less power than the traditional voltage sense amplifier techniques.

This work explores multiple sense amplifiers – Current Sense Amplifier (CSA), Charge Transfer Sense Amplifier (CTSA) and compares them in speed, area, and power to the Voltage Sense

Amplifier (VSA). A current sense amplifier operates by sensing the bit cell current directly rather than waiting on a differential voltage to develop on the bit-lines. The operation of charge transfer sense amplifier is based on charge sharing from the high capacitance bit-lines to the low capacitance sense amplifier node.

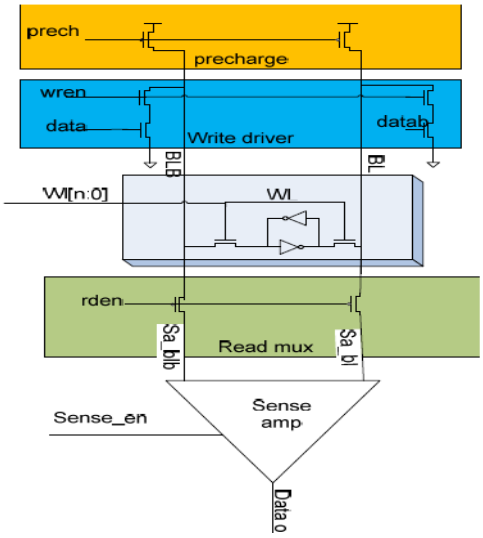

Figure 1: Basic schematic of one column for small signal memory array using 6T cell

Voltage Sense Amplifier

A voltage sense amplifier senses the differential voltage on the bit-lines and generates a full rail output. The circuit is shown in Figure 2

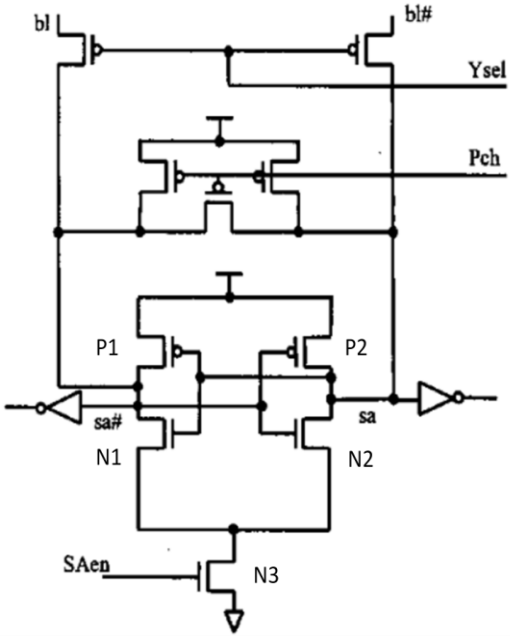

Figure 2: Voltage Sense Amplifier

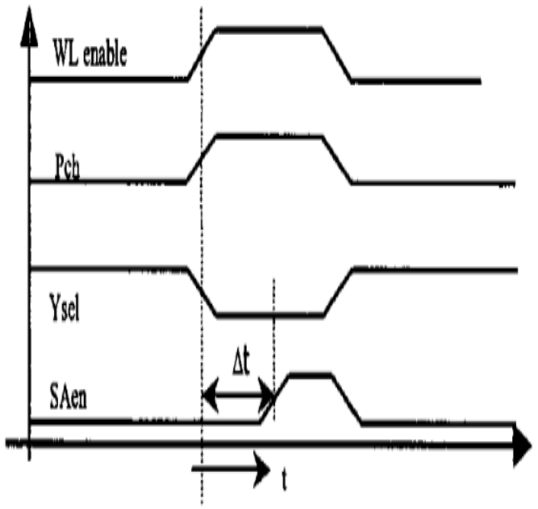

Figure 3: Timing Scheme for a Voltage Sense Amplifier

The operation of the circuit is as follows. When WL is enabled, a voltage differential begins to develop on the bl/bl# pair. When enough differential, depending on the technology and circuit, has developed the sense amp enable (SAEN) is activated which causes the cross coupled inverters to go into a positive feedback loop and translate the differential to full rail output. The sense amplifier output node which connects to the bit-line with a lower voltage, for eg sa, is pulled down to 0 while the other output sa# remains high. When sense amplifier is enabled, NMOS devices N1 and N2 go into saturation. The NMOS device N2 which receives full VDD input has a higher current than N1 with a smaller voltage as its Vgs. The one which conducts higher current (N2) pulls its output voltage lower reducing the Vgs on the other NMOS device (N1), which therefore has smaller current flowing through it.This positive feedback loop continues until the output voltage sa has fallen low enough to cause the NMOS device N2 to enter linear region and turn on the PMOS device P1 of the other inverter and cause its output to be driven high. N1 is eventually turned OFF, and the cross coupled inverters store the resulting output.

Current Sense Amplifier

The current sense amplifier (CSA) operates by sensing the bit cell current directly. It is not dependent on a differential voltage developing

across the bit-lines. This helps reduce bit-line pre-charge power since the low going bit-line can be clamped at a higher voltage than would be required with a voltage sense amplifier. The current sense amplifier consists of two parts: a current transporting circuit with unity gain current transfer characteristics and a sensing circuit which senses the differential current. The circuit diagram of the current sense amplifier is shown in Figure 4. It is designed with a combination of ideas from [1] and [5].

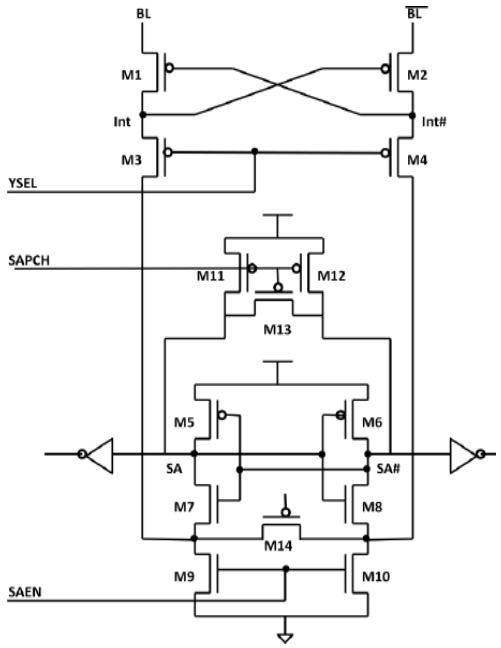

Figure 4: Current Sense Amplifier

The current transporting circuit or the current conveyor consists of four equally sized PMOS transistors (P1 through P4) with positive feedback. These devices operate in saturation. The current conveyor circuit, shown in Figure 5, operates as follows. The gate-source voltage of M1 will be equal to that of M3, since their currents are equal, their sizes are equal, and both transistors are in saturation. Let this voltage be represented by V1. Similarly, the gate-source voltages of M2 and M4 are also equal, let this be

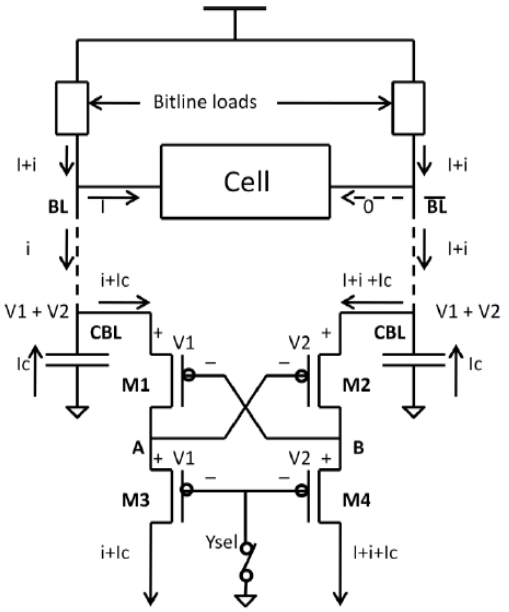

Figure 5: Current Conveyor Circuit

represented by V2. When YSEL is grounded, the voltage on BL is given by V1+V2, so is the voltage on BL#. Therefore, the potential of the bit-lines will be equal independent of the current distribution. This means that there exists a virtual short circuit across the bit-lines. Since the bit-line voltages are equal, the bit-line load currents will also be equal, as well as the bit-line capacitor currents. Since the cell draws a current I, the right leg of the current conveyor draws more current than the left leg. The difference between these two currents will be equal to the cell current. The drain current of M3 and M4 are passed to the current conveyor output which is connected to the current sensing circuit. The differential output current of the current conveyor is therefore equal to the cell current.

The current sense amplifier operates in two phases: precharge and evaluate. During the precharge phase, the bit-lines are precharged through precharge devices connected to the bit-lines (not shown here). The sense amplifier output nodes SA and SA# are also precharged high through M11 and M12 PMOS devices. Devices M11 and M13 are ON during precharge, equalizing the inputs and outputs of the sensing circuit respectively. The operating current of the sense amplifier is determined by the sizes of devices M5-M8. At the end of the precharge

phase, precharge and equalization devices M11-M14 are turned OFF. During the evaluation phase, YSEL is pulled low and SAEN is pulled high. The cross coupled inverters comprising of devices M5-M8 then form a high gain positive feedback amplifier. Due to the positive feedback, the impedance looking into the source terminal of either M7 or M8 is a negative resistance, which causes M7 and M8 to begin sourcing a portion of the difference current. The difference current flowing through M7 and M8 flows through the small equivalent capacitance at the drains of M7 and M8, giving rise to a voltage difference across the output nodes of the sense amplifier. The initial trajectory for the magnitude of the voltage difference between the drains of M7 and M8 is given by

$$d\Delta V/dt = 2\Delta I/Cd$$

where Cd is the total capacitance at the drain node of M7 or M8. This trajectory is followed for a short time, and then the resulting differential voltage at the output of the sense amplifier is rapidly amplified by the positive feedback of the cross coupled inverters, driving one output to zero and keeping the other one high.

The sensing delay is relatively insensitive to bit-line capacitance as the operation is not dependent on the development of a differential voltage across the bit-lines. Unlike the voltage sense amplifier, the output nodes are not tied to the high capacitance bit-lines and are able to respond very quickly. The CSA can have lower voltage swing on bit-lines. This is because the cross coupled PMOS pair M1 and M2 cuts off the discharge path to ground for both bit-lines. Suppose BL is high and BL# is going low. This causes nodes Int and A to go high causing M2 to be cut off. Therefore, the path from the low going BL# to ground is cut off, reducing the voltage swing on it.

Charge Transfer Sense Amplifier

The Charge Transfer Sense Amplifier (CTSA) operates by making use of the charge redistribution from high capacitance bit-lines to the low capacitance sense amplifier output nodes. This results in high speed operation and lower power consumption due to low voltage swing on the bit-lines. The circuit diagram of a CTSA is shown in Figure 6.

The basic concept behind charge-transfer amplification is to produce voltage gain by exploiting charge conservation among capacitive devices. For a series connection of two capacitive elements in a system for which charge is conserved, the product of the voltage across the first element and its capacitance must equal the product of the voltage across the second element and its capacitance as shown in the following equation.

$$C_{small} V_{small} = Q = C_{large} V_{large}$$

Voltage gain is therefore realized since a small change in voltage across the larger capacitive element will produce a larger change in voltage across the smaller capacitive element.

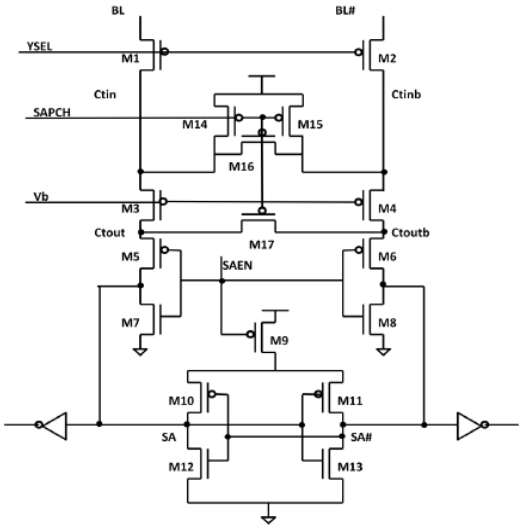

Figure 6: Charge Transfer Sense Amplifier

The operation of CTSA circuit is based on the charge redistribution from high bit- line capacitance to the low capacitance of sense nodes sa and sa#. This charge redistribution results in high speed operation and low bit-line swing. The circuit consists of two parts. First is the common gate cascode formed by M3, M5 and M7 (and M4, M6 and M8), with PMOS devices M3 and M4 biased at Vb. Second, the cross-coupled inverters formed by M9 and M13, latches the output of the common-gate amplifier (Sa and Sa#).In the precharge phase, the bit-lines and all the intermediate nodes (ctin, ctinb, ctout, ctoutb) are precharged high. The output of

the common gate amplifier (sa and sa#) are predischarged low by keeping SAen high. In the evaluation phase, SAPCH is pulled high and YSel is grounded to select a column. CTSA is enabled by pulling SAen low. Suppose the bit-line bl# is going low. As the voltage of bl# goes near Vb + Vtp, M4 goes into sub-threshold region of operation preventing the output node sa# from getting charged. However, the other bit-line bl remains high and charges the output node sa to high. Initially NMOS pair M12 and M13 helps in rejecting the common mode noise and thereafter helps in latching the value sensed by the common gate amplifier. The timing scheme of the CTSA is shown in Figure 6.

Conclusion

Current sensing is typically faster than voltage sensing. Current sense amplifier can be enabled faster than voltage mode, as current sensing does not depend on differential discharging of large bit-line capacitance. The bitline swing for current sensing is less than the voltage mode, but the energy saved with reduced bit-line swing is compensated by the static power dissipation of the current sense amplifier. Charge transfer sense amplifier offers both speed and power advantage. CTSA is faster than the voltage mode sense amplifier. CTSA consumes lower energy than voltage mode sense amplifier. The bit-line swing for CTSA is at least lower than voltage mode counterpart and this gives a quadratic saving of about in the energy. CTSA is as robust as voltage mode with respect to Vt mismatch. CTSA offers dual advantage of high-speed and low energy. However, CTSA suffers from the additional complexity in the design of bias voltage generator. We are further studying the impact of the secondary design issues like Vt mismatch, bit-line capacitance mismatch etc. To determine the robustness of these two circuits.

References

1. Travis N. Blalock and Richard C. Jaeger. A High-Speed Clamped Bit-Line Current-Mode Sense Amplifier. IEEE JSSC, Vol 26, No 4, April 1991.
2. Evert Seevinck, Petrus J. van Beers and Hans Ontrop. Current-Mode Techniques for High-Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAMs. IEEE JSSC, Vol 26, No 4, April 1991.
3. Shoichiro Kawashima, Toshihiko Mori, Ryuhei Sasagawa, Makoto Hamaminato, Shigetoshi Wakayama, Kazuo Sukegawa and Isao Fukushi. A Charge-Transfer Amplifier and Encoded-Bus Architecture for Low-Power SRAMs. IEEE JSSC, Vol 33, No 5, May 1998.
4. Tsuguo Kobayashi, Kazutaka Nogami, Tsukasa Shirotori, and Yukihiro Fujimoto. A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture. IEEE JSSC, Vol 28, No 4, April 1993.
5. Sandeep Patil, Michael Wieckowski and Martin Margala. A Self-Biased Charge-Transfer Sense Amplifier . IEEE, 2007.
6. Manoj Sinha, Steven Hsu, Atila Alvandpour, Wayne Burleson, Ram Krishmamurthy and Shekhar Borkar. High-Performance and Low-Voltage Sense Amplifier Techniques for sub-90nm SRAM. IEEE, 2003.
7. Shin-Pao Cheng and Shi-Yu Huang. A Low-Power SRAM Design Using Quiet-Bitline Architecture. IEEE MTDT ’05.
8. Tsuguo Kobayashi, Kazutaka Nogami, Tsukasa Shirotori and Yukihiro Fujimoto. A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input.